Stack Height Analysis for FinFET Logic and Circuit

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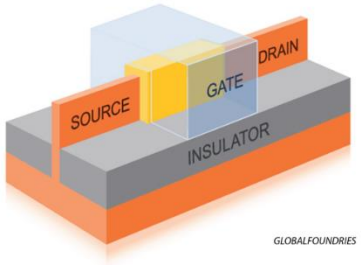


Outline

- Background & Motivation
- FinFET Design and Simulation Flow
- Stack Height Analysis
- A Case Study: A 64-bit Adder
- Conclusion & Future Work

FinFET (Tri-gate)

- Superior levels of scalability
- Relatively easy for fabrication
- Reduction of leakage
- Faster than the non-FinFET versions

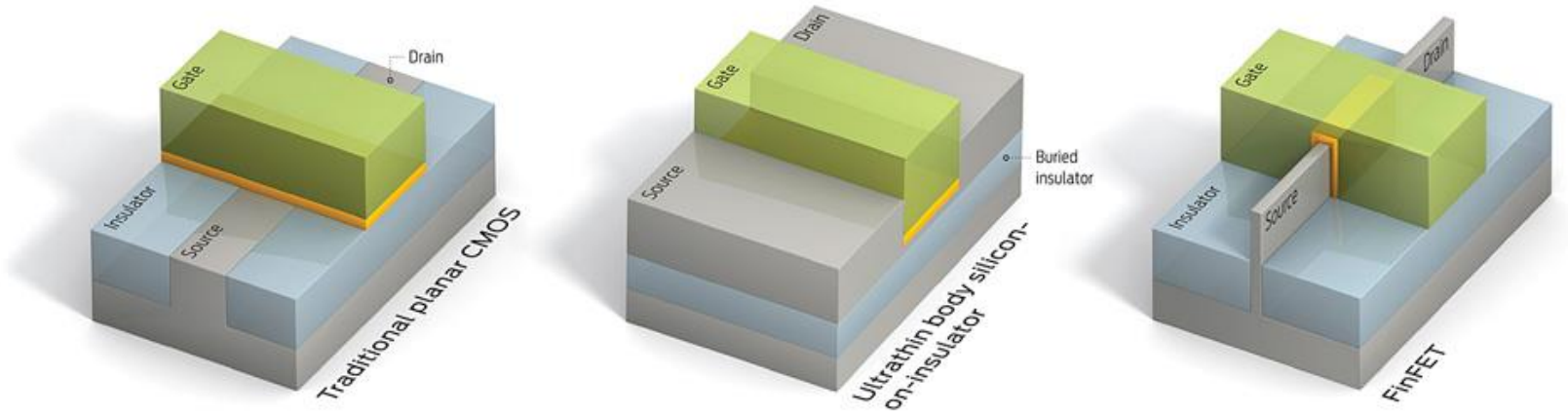


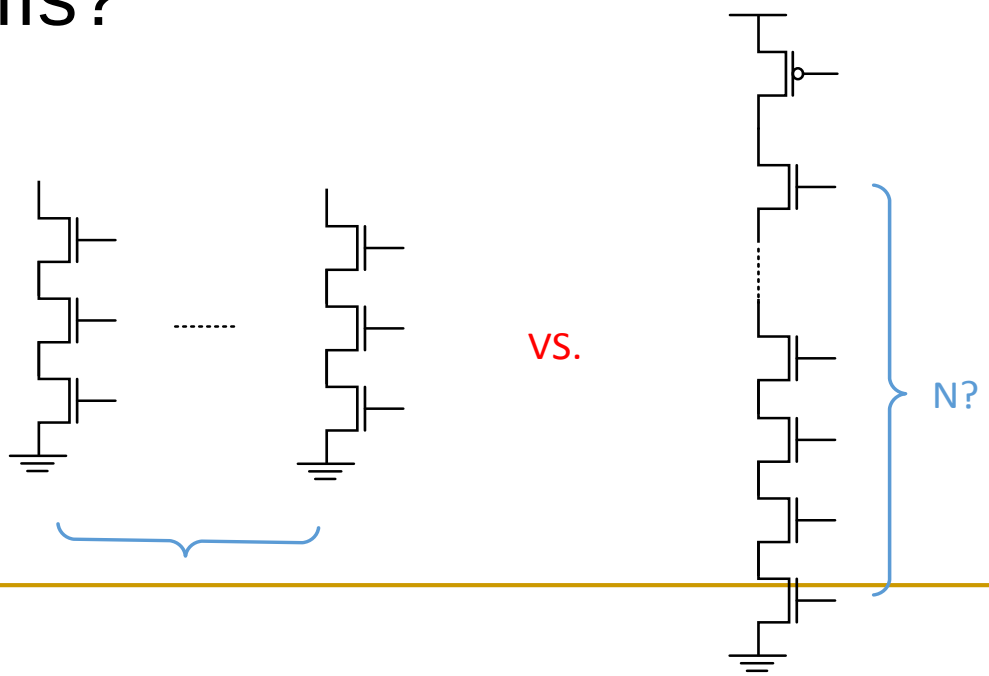
Figure: K. Ahmed et al. "Transistor Wars - Rival architectures face off in a bid to keep Moore's Law alive" *IEEE Spectrum*, 2011

Some Challenges of FinFET

- Width Quantization
- Watch your PDN and EM!
- Thermal Issues, Reliability Challenges
- Complex Gate Cap model
- Gear ratios (metal pitch vs. fin pitch)
- Little/No Body Effect → More complex cells / Higher fan-in
- …

Research Questions

- Can we utilize this unique property to reduce the *logic depth* by increasing *fan-in*, thus improve performance?
- How many can we stack? What are the tradeoffs?



Previous Research

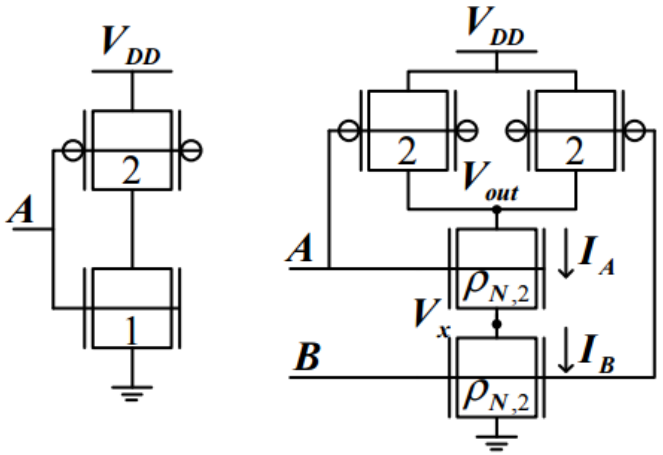
- The stack depth of 2 is highly preferred for FinFET circuit designs in the sub/near-threshold region.

V_{DD}		16-input AND		256-input AND		4096-input AND		
	Stack depth	2	4	2	4	2	3	4
0.3V	Area	160	212	2720	3604	43680	47697	57876
	Delay (ns)	0.0463	0.0480	0.0958	0.1031	0.1452	0.1496	0.1578
	ADP	7	10	261	372	6342	7135	9133
0.25V	Area	170	232	2890	3944	46410	52308	63336
	Delay (ns)	0.0787	0.0803	0.1647	0.1753	0.2503	0.2527	0.2702
	ADP	13	19	476	691	11616	13218	17113

X. Lin et al. “Stack Sizing Analysis and Optimization for FinFET Logic Cells and Circuits Operating in the Sub/Near-Threshold Regime”, ISQED, 2014

Previous Research (cont'd)

- Based on their own model
- In near/subthreshold region
- Ignore wire capacitance
- P/N Drive Strength 2:1

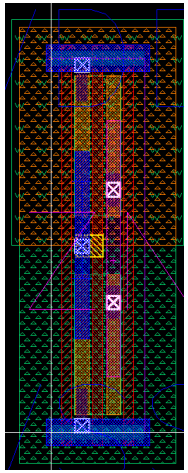


X. Lin et al. "Stack Sizing Analysis and Optimization for FinFET Logic Cells and Circuits Operating in the Sub/Near-Threshold Regime", ISQED, 2014

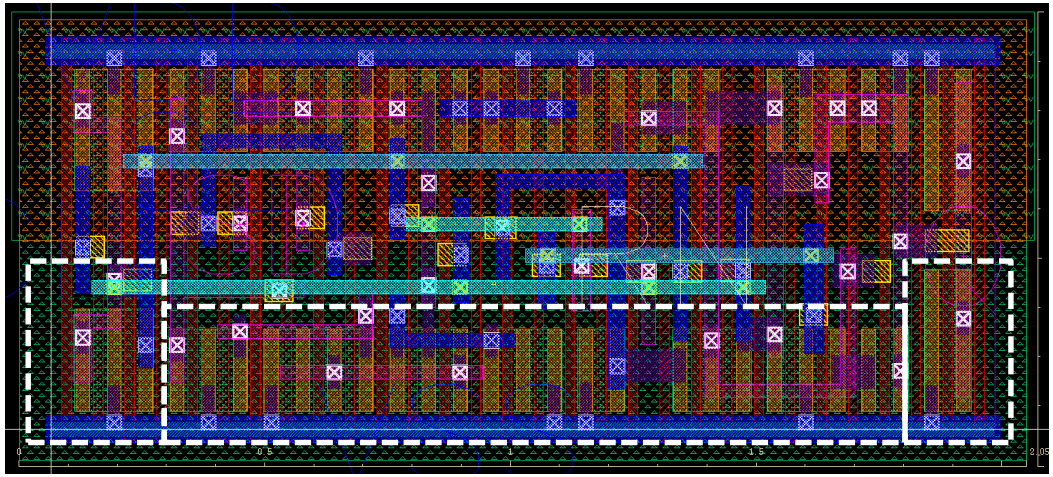
FinFET FreePDK15

- Physical Design
- Layer Information, DRC works
- NanGate Cell
- No LVS rules and Models

P/N = 1/1



INVX1

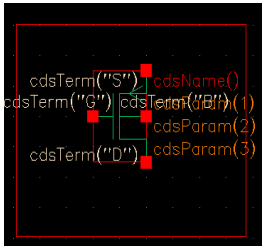


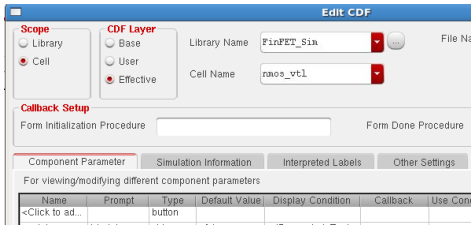
SDFF

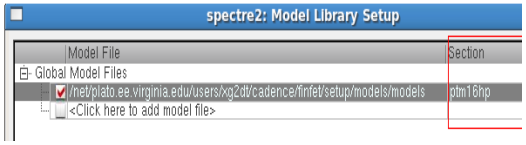
Simulation Flow

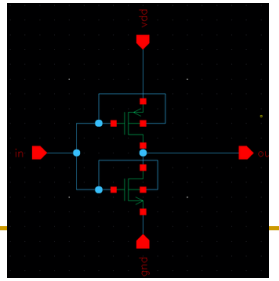
- Model: PTM Model (5 Technology Nodes)
- Simulation Flow: HSPICE or Spectre

Create Symbol → Modify CDF Parameter → Include Model



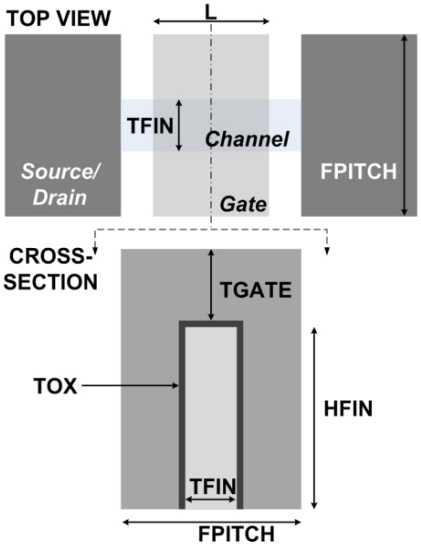






PTM Model

- 72 Levels
- 4 Terminals (1 Floating)
- No body effect
- Sizing -> Change m

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* Temporary parameter list file for ITRS 2011 ver2 models
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.param vddp=-0.9
.param fin_height=28n
.param fin_width=15n
.param lg=24n
.endl

.lib 16nm
.param vdd=0.85
.param vddp=-0.85
.param fin_height=26n
.param fin_width=12n
.param lg=20n
.endl

.lib 14nm
.param vdd=0.8
.param vddp=-0.8
.param fin_height=23n
.param fin_width=10n
.param lg=18n
.endl

.lib 10nm
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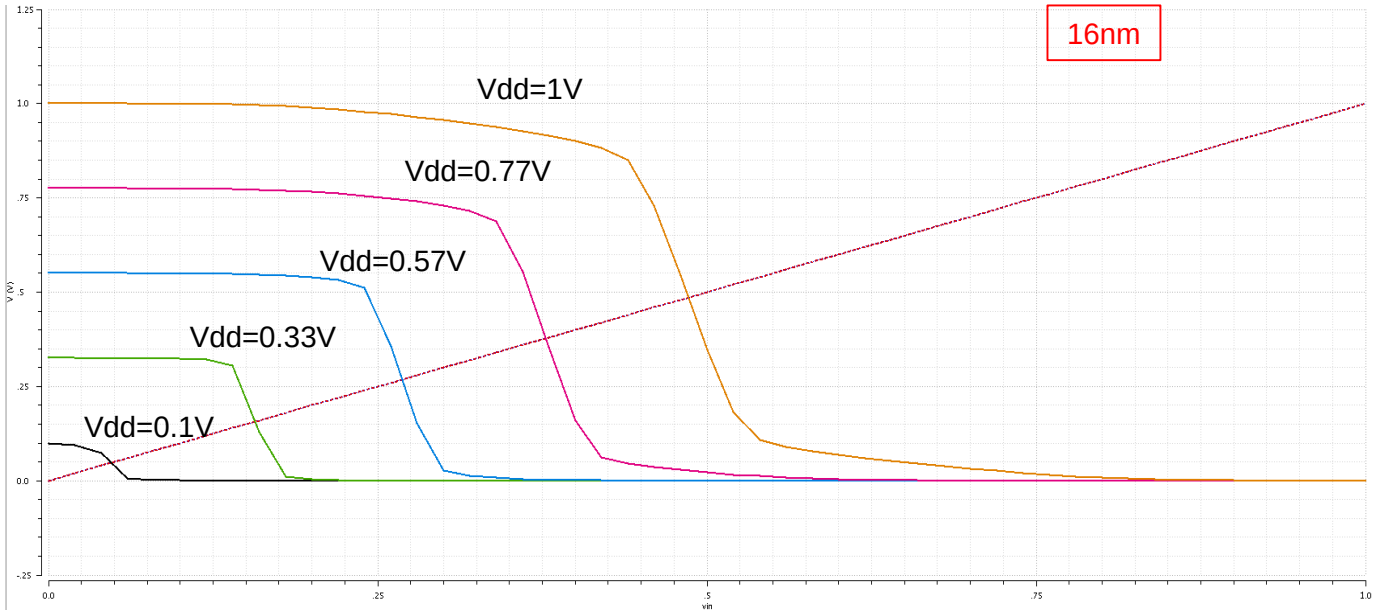
.param vddp=-0.75
.param fin_height=21n
.param fin_width=9n
```

http://ptm.asu.edu/

Sinha, Saurabh, et al. "Exploring sub-20nm FinFET design with predictive technology models." DAC, 2012

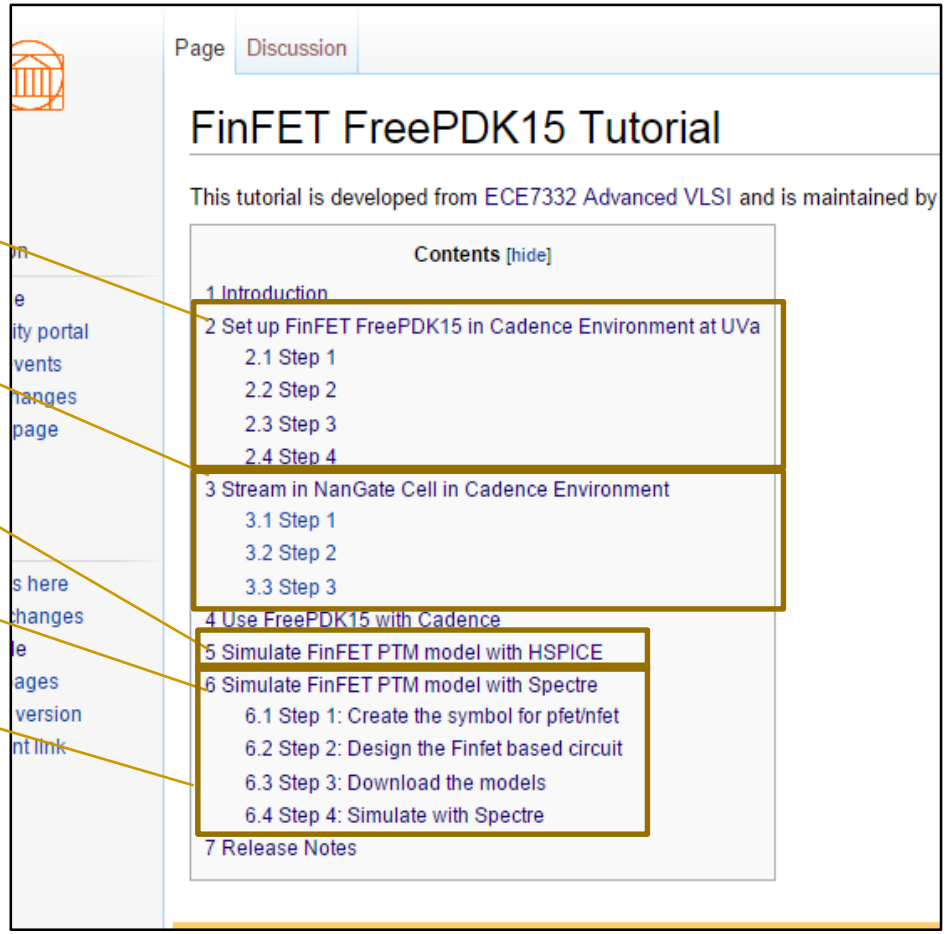
Characterize the model

- An invert driving FO4 as load
- P/N=1:1
- tplh=49.9ps, tphl=45.16ps



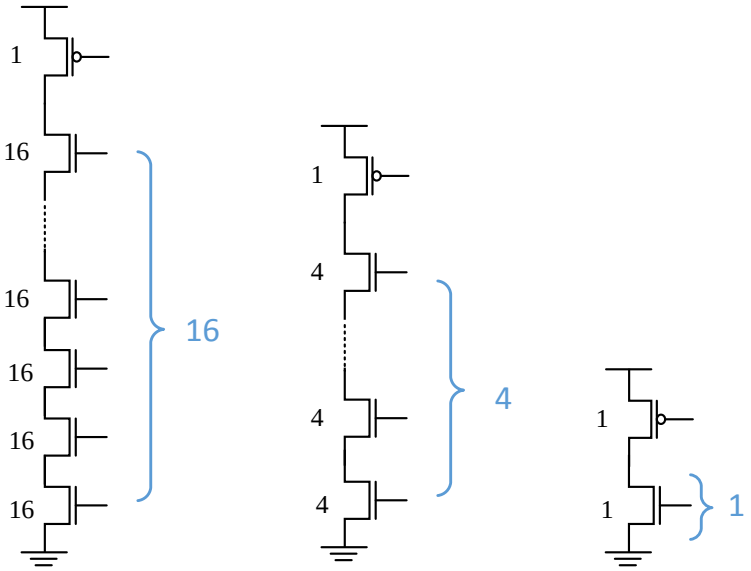
FinFET FreePDK Tutorial

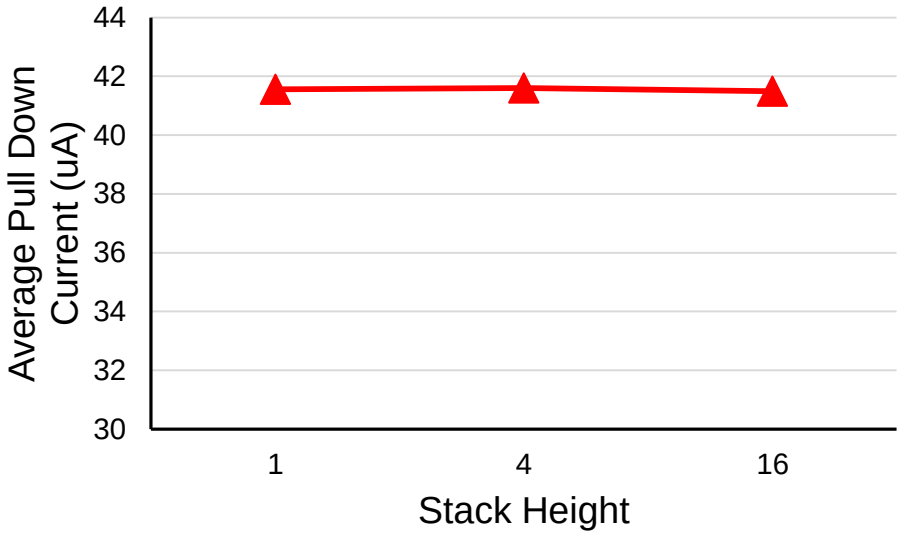
- Setup
- Layout
- HSPICE
- Spectre/UltraSim
- use ocean script



Body Effect?

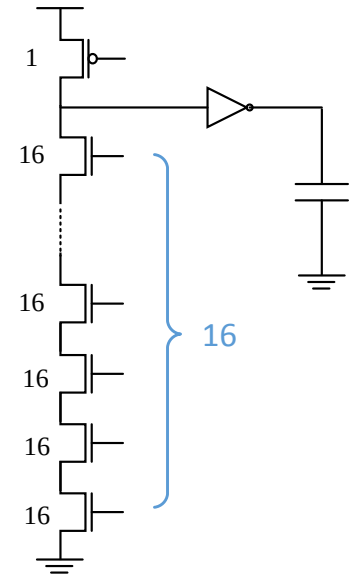
- P/N=1:1 16nm
- Test Circuit: NAND, load cap=5fF
- Average Pull Down Current



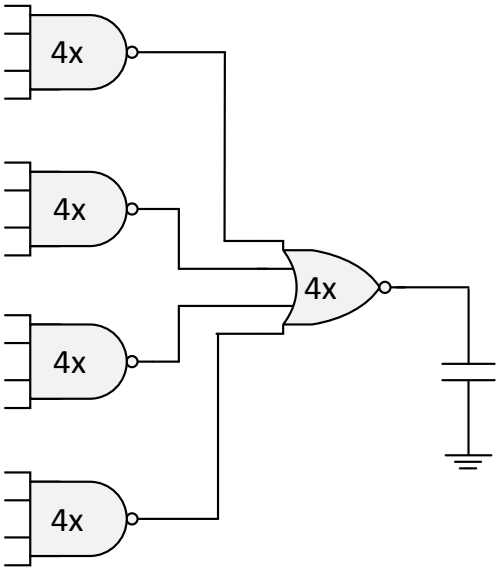


16-AND Gate

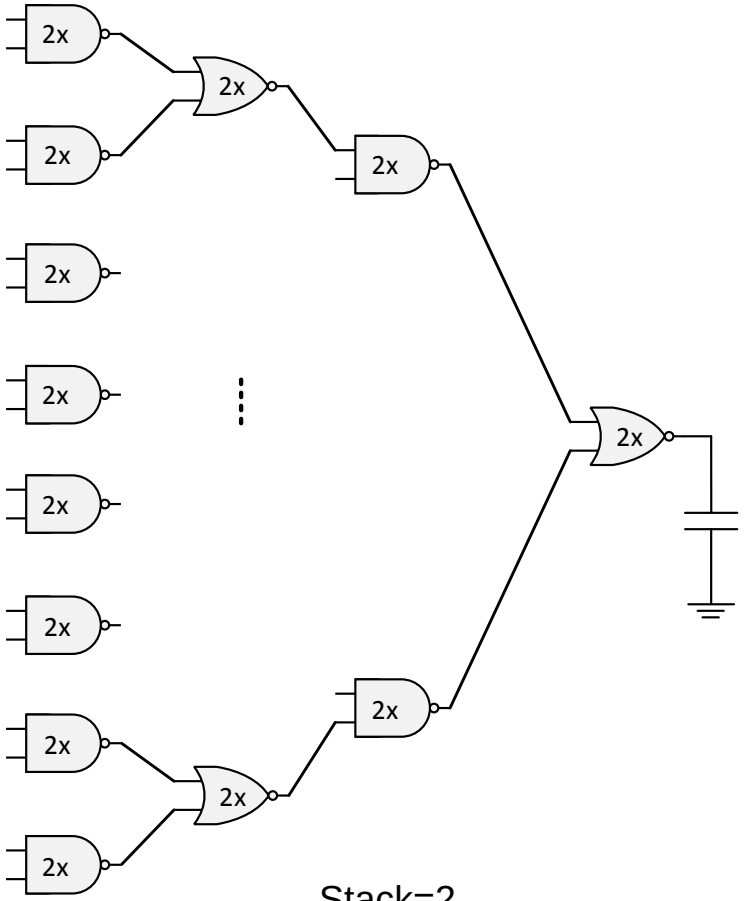
- P/N = 1:1



Stack=16



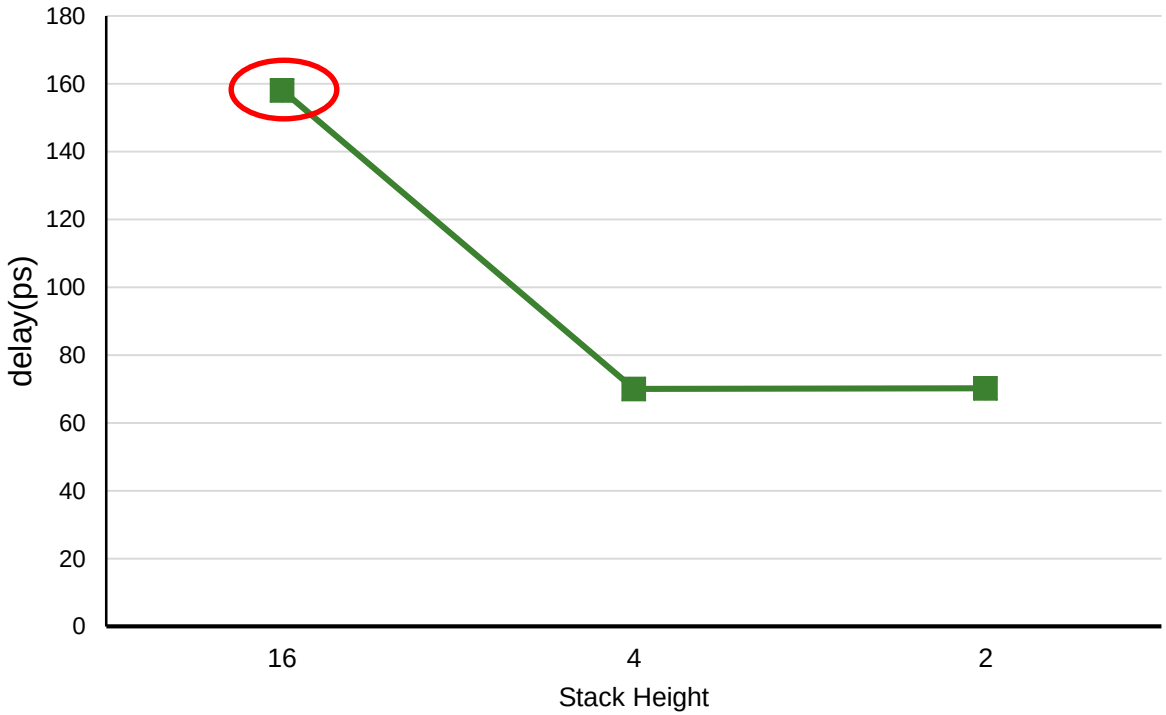
Stack=4



Stack=2

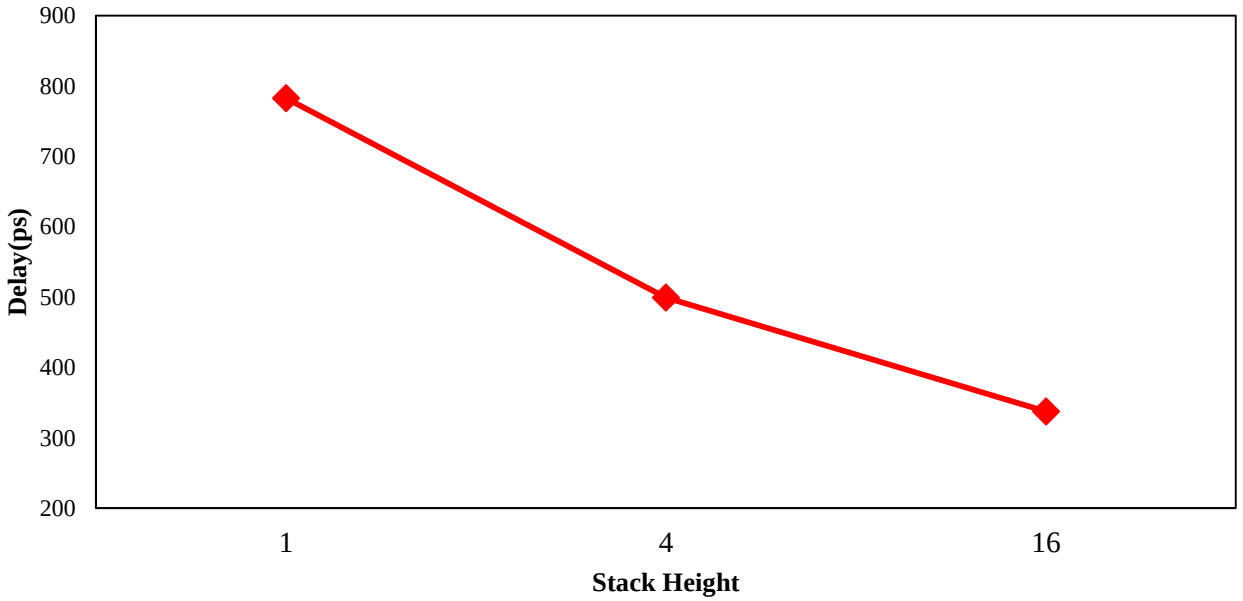
Simulation Result

- Slow!



Wire Cap!

Add a cap at each internal node. Cwp=50fF

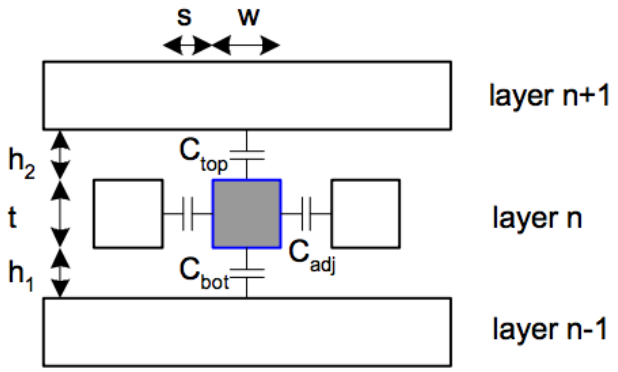


When wire cap dominates, higher stack design has a much better performance.

Is 50fF reasonable?

- Wire Capacitance
- Coupling Cap
- PTM Interconnect Calculator

$$C_{total} = C_{top} + C_{bot} + 2C_{adj}$$



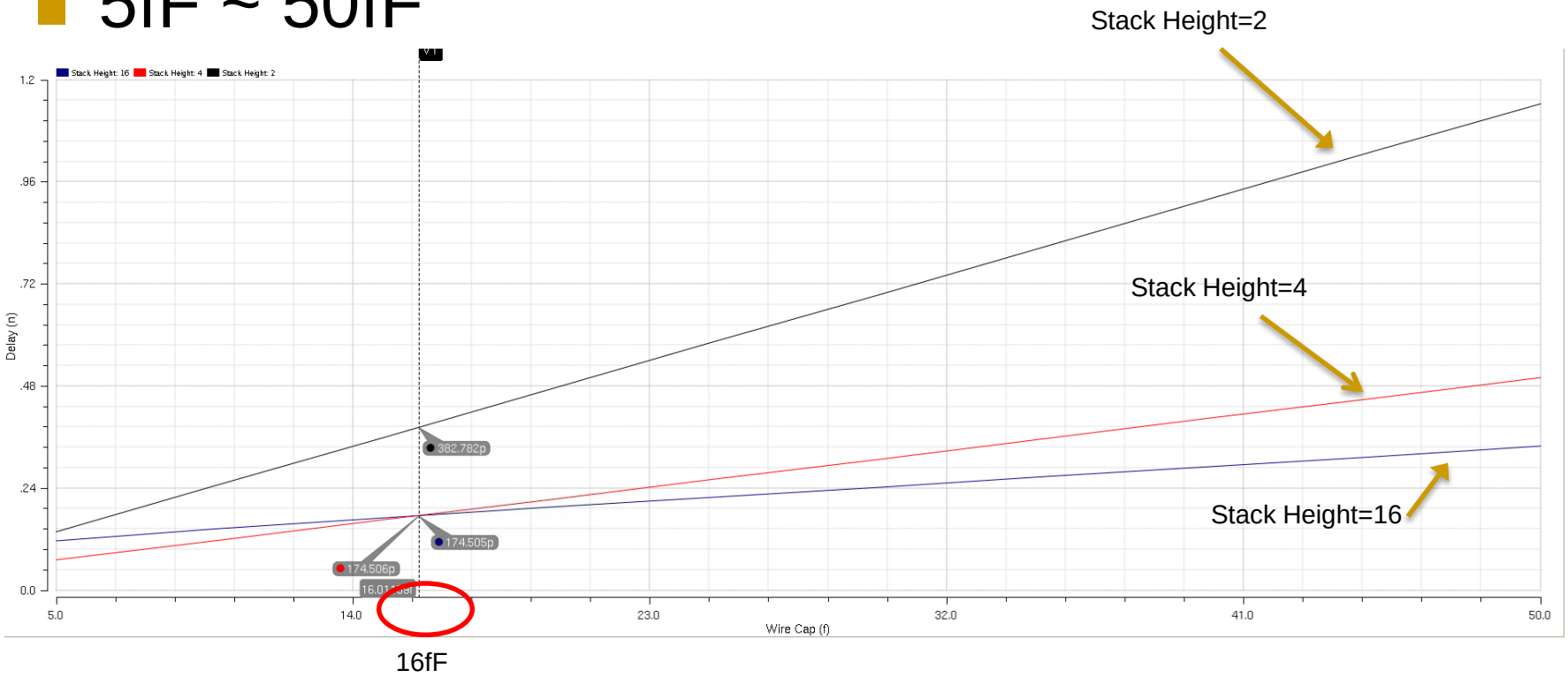
N. Weste and D. Harris, “CMOS VLSI Design”

Dimensions	RLC
W = 0.050 um s = 0.050 um l = 5 um t = 0.20 um h = 0.20 um K = 2.2	R = 10.999 Ohm L = 0.004 nH M12 = 0.003 nH M13 = 0.002 nH M14 = 0.002 nH (k12 = 0.75 k13 = 0.5 k14 = 0.5) Cground = 0.04746 fF Ccouple = 0.56906 fF Ctotal = 1.23304 fF

http://ptm.asu.edu/

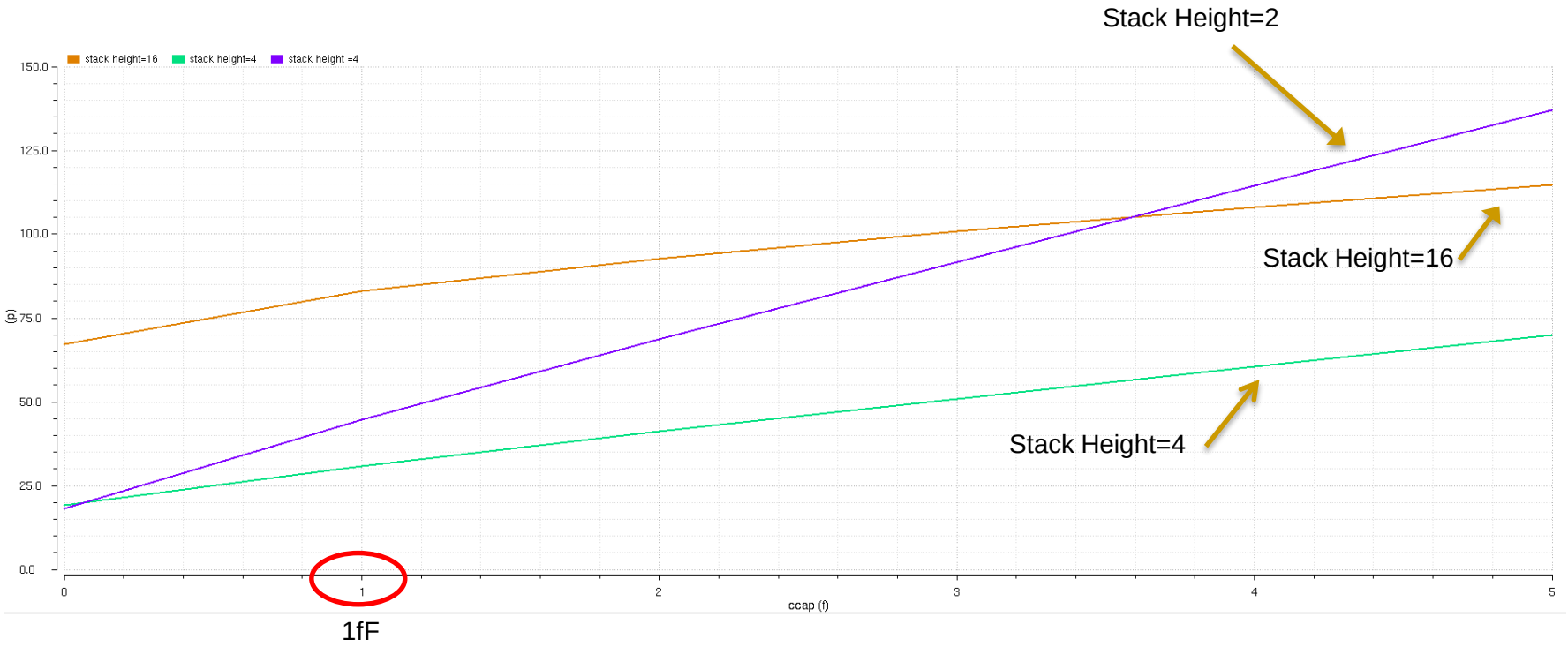
Delay vs. WireCap

- 16-AND Gate
- 5fF ~ 50fF



Delay vs. WireCap

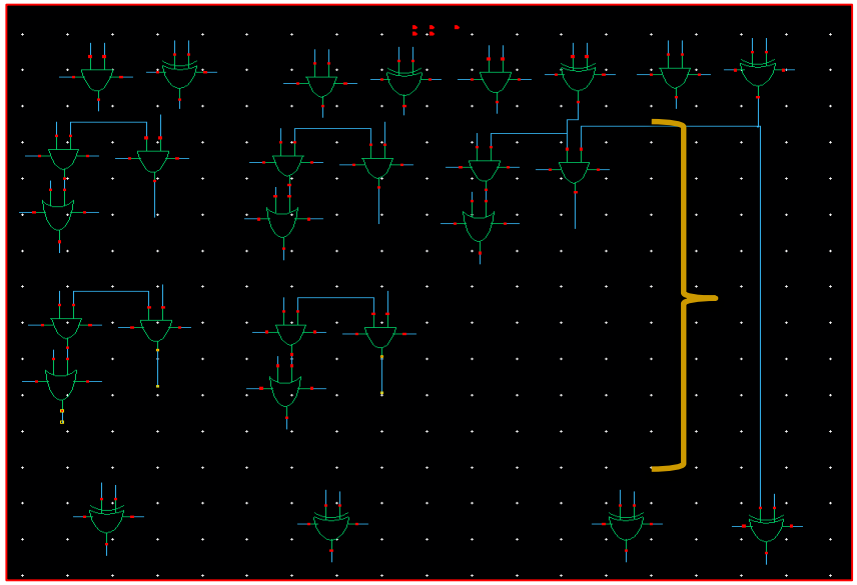
- 0-5fF



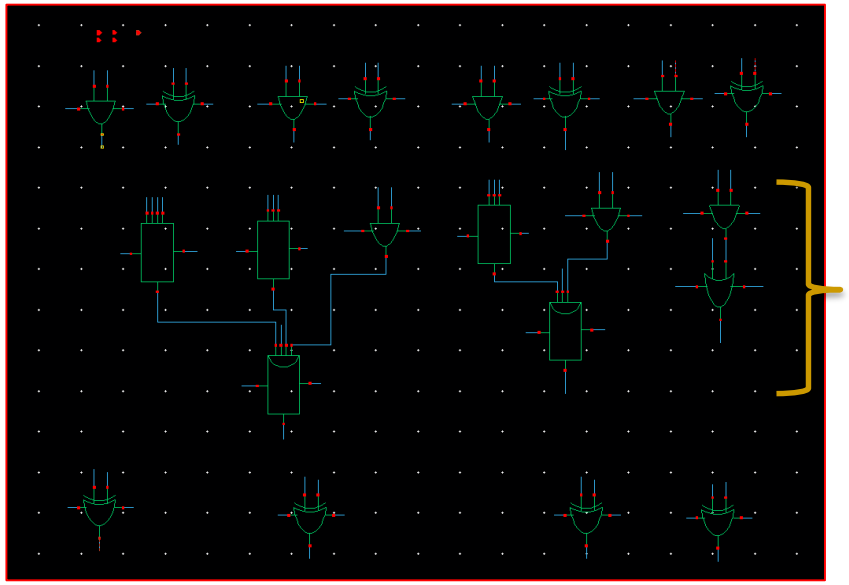
There must be an optimal stack height if accurate wire cap estimation is given.

4-bit Look Ahead Adder

- Radix-2 KSA: 26.84ps
- Radix-4 KSA: 29.89ps



Radix-2



Radix-4

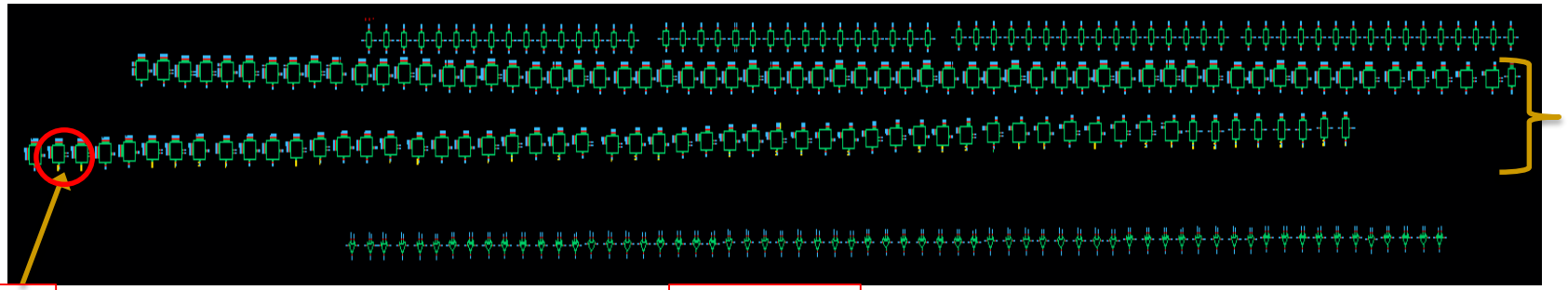
16nm

Radix-4 is still slower? Why?

Gate Cap vs. Stack Height

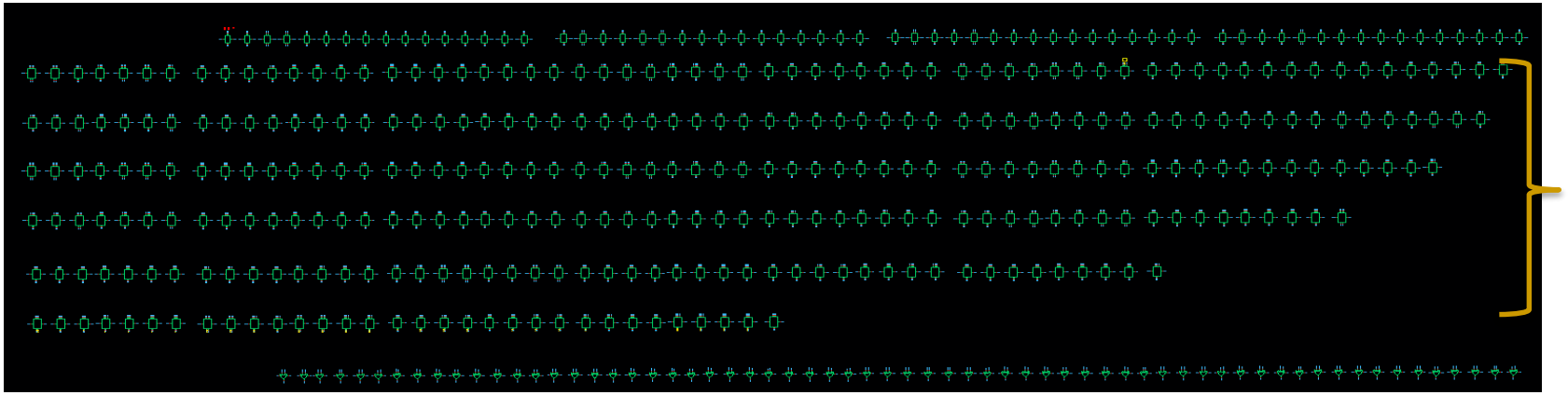
- As we increase the stack size while keeping the same drive strength, size is increased proportionally.
- Tradeoff: Driven Gate Capacitance vs. Stack Height
- Wire Cap is not considered in this case

64-bit Kogge-Stone Adder



8 inputs

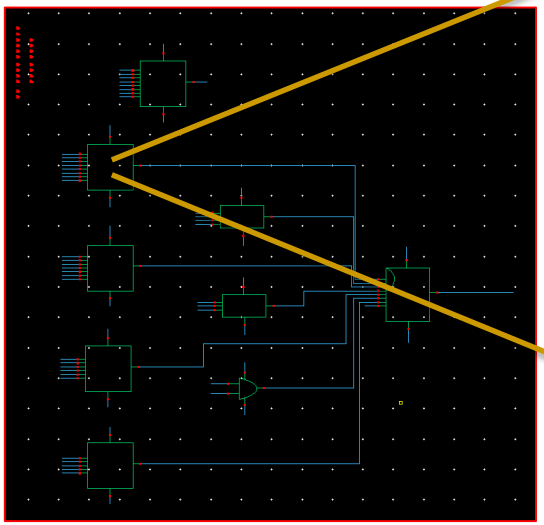
Radix-8



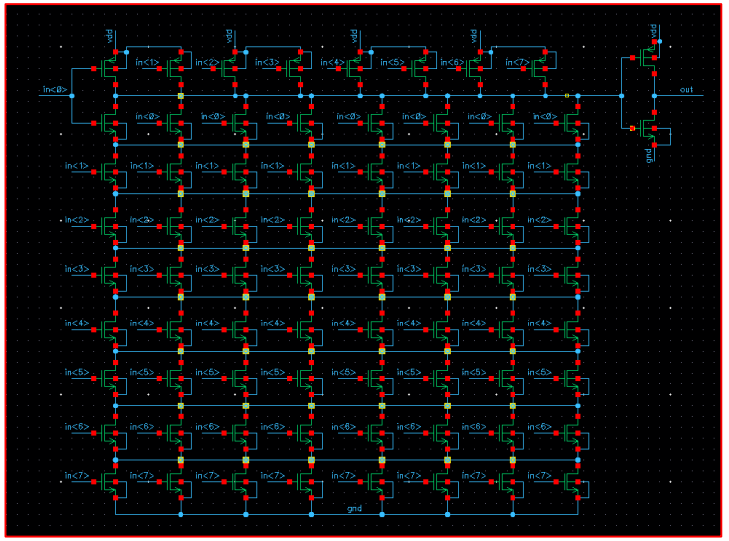
Radix-2

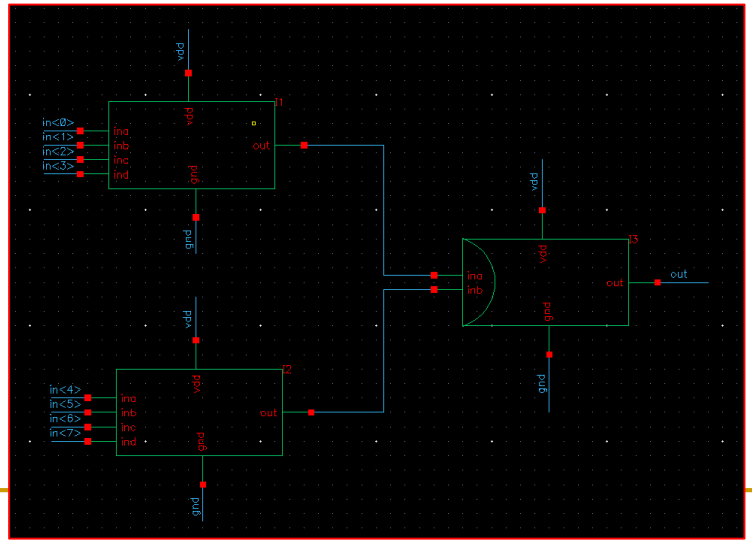
1 Stage vs. 2 Stages

- 1 Stage -> Total: 4 Stages
- 2 Stages -> Total: 8 Stages
- Radix 2 -> Total: 12 Stages

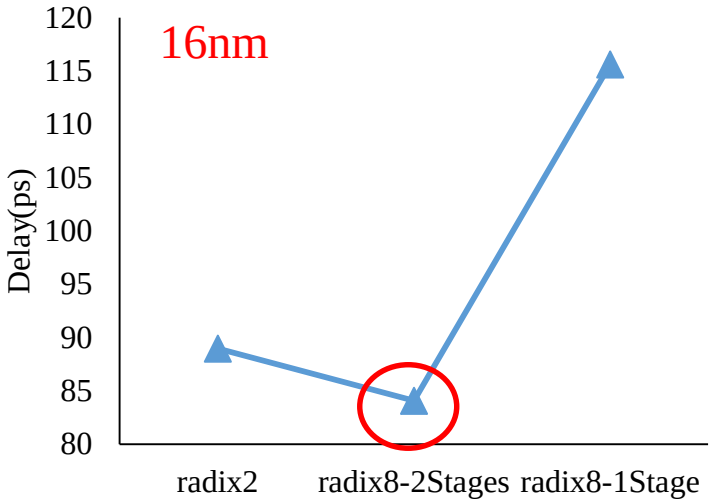


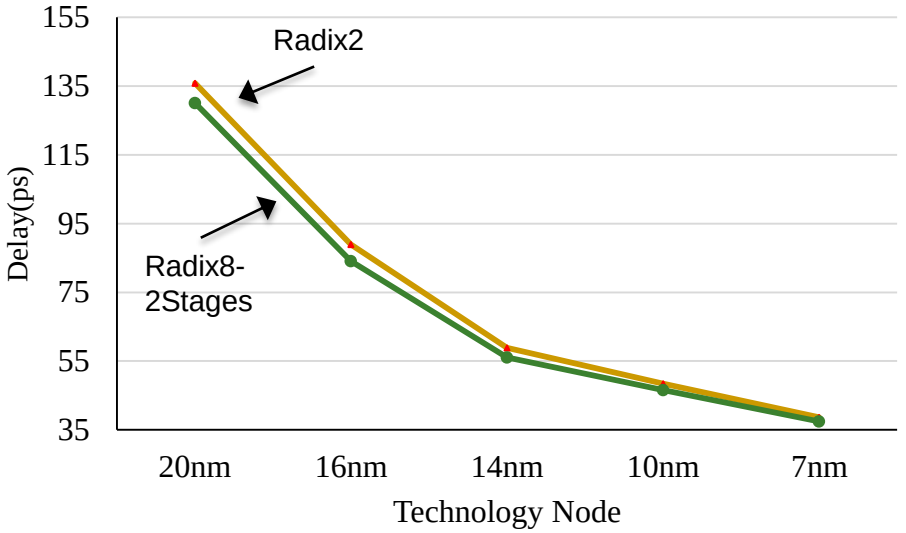
OR

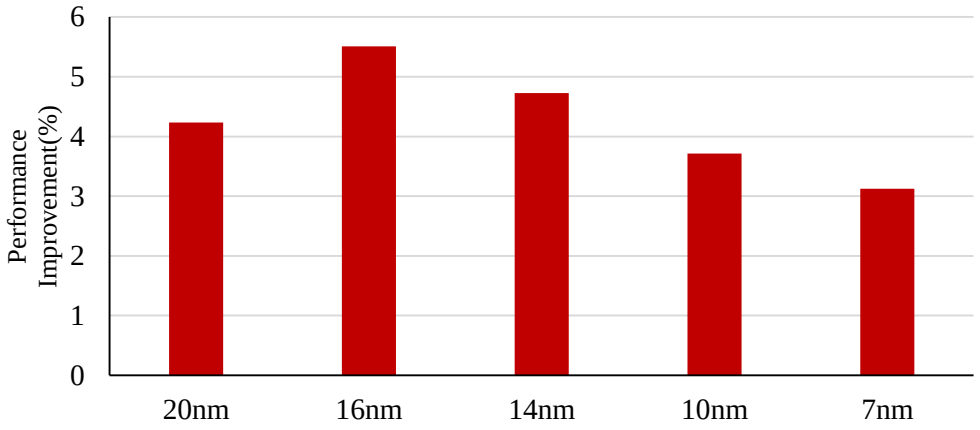




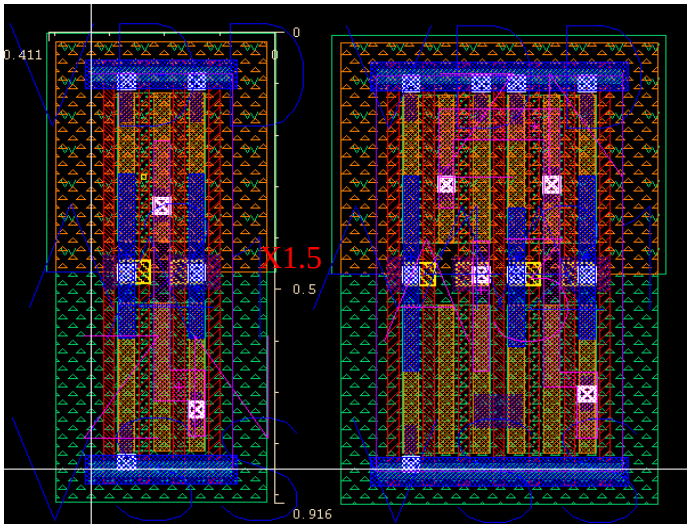
Simulation Result



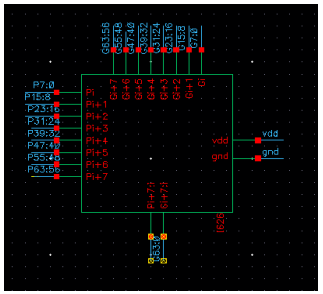




Area Overhead?

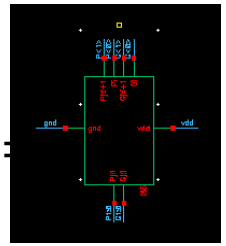


NAND2x1 NAND4x1



#: 100

= 5X

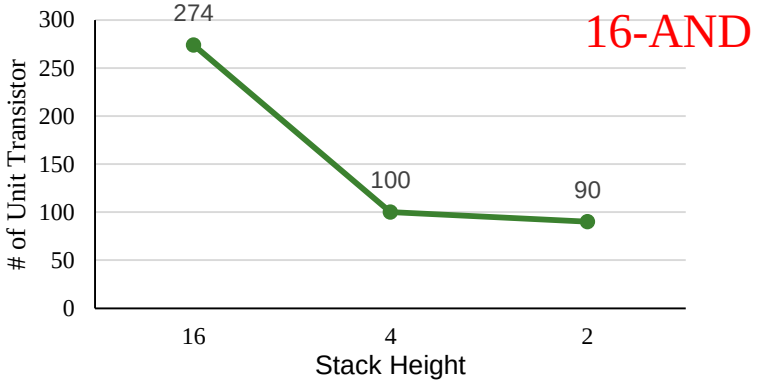


#: 321

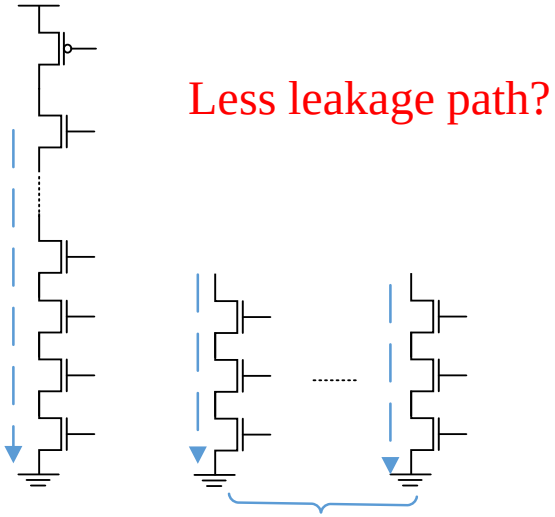
The area is roughly 1.5 larger!

Tradeoffs

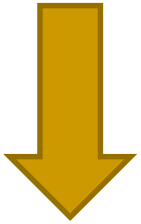
- Area vs. Stack Height



- Leakage vs. Stack Height
- Gate cap vs. Stack Height



Design flow



Fair estimation of the interconnect cap → Decide design metrics (area, leakage..) → Find the optimal stack height

Conclusion

- Higher Fan-in FinFET design has potential of increasing performance
- At design phase, fair assumptions of wire cap are necessary.
- Adder Case Study: There is an optimal stack height
- Design Tradeoffs
- A post-layout simulation is necessary !!!

Discussions

- What if we don’t always keep P/N=1:1? tradeoff between Gate cap vs. Drive Strength?
- 3D-FinFET IC? Pros & Cons?

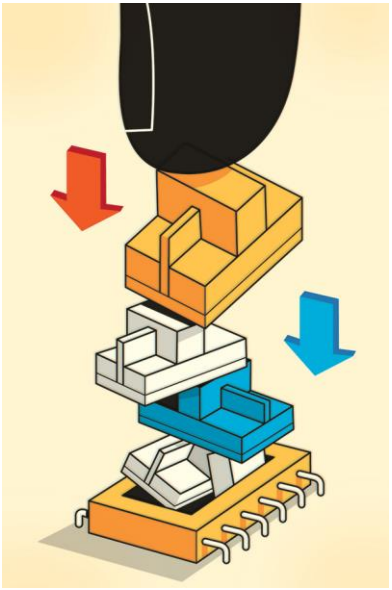


Illustration: Harry Campbell

Thank you!

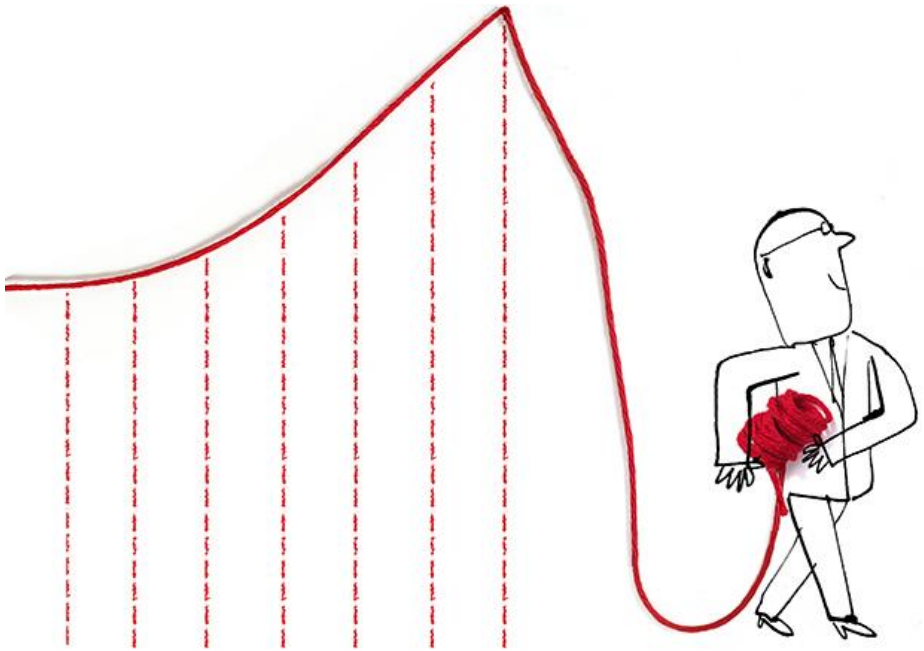


Illustration: Serge Bloch

A. Huang, “The Death of Moore’s Law Will Spur Innovation”, IEEE Spectrum, 2015